* U F - 8 0 6 3 *

UF-8063

B. E. - II (Sem. - III) (Computer) Examination

May\June – 2012

Computer Organization & Architecture

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - II (Sem. - III) (Computer)

Name of the Subject :

☛ Computer Organization & Architecture

☛ Subject Code No. : 8 0 6 3 ☛ Section No. (1, 2,.....) : 1,2

Seat No. :

Student's Signature

(2) Figures to extreme right indicate maximum marks.

(3) Make necessary assumptions and clearly mention them, if required.

(4) Support your answers with block diagram or neat sketches, if required.

SECTION - I

1 (a) Answer the following questions : **10**

(i) Are all micro programmed computers also microporcessor? State your views. **2**

(ii) Write register transfer statement to set the interrupt flip-flop R to 1. **2**

(iii) How many references to memory are needed for Direct and Indirect instruction ? **2**

(iv) Define pseudo instruction. **2**

(v) State the use of the following registers : **2**

(a) PC

(b) IR.

(b) Answer the following questions : **10**

(i) What is three state buffer ? Explain hardware implementation of common bus with three state buffers. **6**

(ii) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored **4**

in one word of memory. The insturction has four parts :
an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(a) How many bits are there in the operation code, the register code part and the address part ?

(b) Draw the instruction word format and indicate the number of bits in each part.

2 (a) Explain Input - Output configuration. **5**

(b) (i) Draw Block diagram of hardwire control unit. Also explain how does it determine type of instruction and execute. **6**

(ii) Draw and explain hardware implementation for 4-bit binary incrementer using full adder. **4**

OR

(b) Draw flowchart for second pass of assembler and explain in detail. **10**

3 Answer the following : (any **three**) **15**

(i) Explain in brief microprogrammed contol organization.

(ii) Write an assembly language program to Add Two Numbers.

(iii) Write microoperation for the BSA memory reference instruction and briefly explain with example.

(iv) Differentiate direct and indirect instructions with example.

SECTION - II

4 (a) Answer the following questions. Each question carried **One** mark. **10**

(i) Define Indexed Addressing Mode.

(ii) Name the processor in which large number of complex instructions are available.

(a) RISC (b) CISC

(c) hardwired (d) microprogrammed

(iii) Define One-Address Instructions.

(iv) Convert the following into reverse polish notation.
A*[B+C*(D+E)] / [F+G*(H+I)]

(v) The addressing mode used in an instruction of the form ADD X Y is _____.

(vi) In a program using sub routine call instruction it is necessary to clear the instruction register. (True/False)

(vii) Floating point representation is used to store
(a) Boolean values (b) whole numbers
(c) real integers (d) integers

(viii) Define pipeline processing.

(ix) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers. (True/False)

(x) RISC is a microprogrammed control unit architecture. (True/False)

(b) Answer the following : (any **two**) **10**

(i) Explain :
(1) Vector Processing.
(2) Vector Operations.

(ii) What is a Memory Stack ? Explain with the help of neat diagrams.

(iii) A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved ?

5 Attempt the following :

(a) List the important characteristics of RISC architecture and explain the use of overlapped register windows. **7**

(b) What is Instruction Pipeline ? Explain the Four-Segment Instruction Pipeline with the suitable diagram. **8**

OR

(b) What are the pipeline conflicts ? Explain the hardware techniques to handle the branch instructions. **8**

6 Attempt the following :

(a) Explain Program Interrupts. Explain clearly, discussing the role of stack, PSW and return from interrupt instruction, how interrupts are implemented on computers. **7**

OR

(a) Explain with proper block diagram the Multiplication Operation on two floating point numbers. **7**

(b) Multiply the (-8) with (12) using Booth's algorithm. Give each step. **8**